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RADIO FREQUENCY SYSTEMS

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MILLIMETER WAVES STUDY

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PREPARED BY

MICROWAVE RESEARCH LABORATORY

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GEORGE C. MARSHALL SPACE FLIGHT CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
HUNTSVILLE, ALABAMA

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FOREWORD

The information contained in this report summarizes the progress made by the Electrical Engineering Department under the auspices of the Auburn Research Foundation of Auburn University toward the fulfill-ment of the requirements prescribed in NASA contract NAS8-11184.

Monthly reports have been submitted prior to this writing. Progress has also been reviewed by telephone and in meetings with Mr. T. A.

Barr, Contract Supervisor, National Aeronautics and Space Administration, Huntsville, Alabama and the personnel at Auburn University.

The following personnel have actively participated on this project during this reporting period:

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I. INTRODUCTION

A new amplifier-filter for use in triggering the oscilloscope in the ground station of the radar altimeter instrumentation system has been built and tested. A manual describing the operation and the calibration procedure for the entire system has been prepared.

Design work has begun on a solid-state 2280 megacycle television exciter. The progress of the design work of this exciter unit is included in the second section of this report.

The progress of the millimeter wave study is included in the third section of this report.

II. RADIO FREQUENCY SYSTEMS

A. Radio Frequency Systems

1. Ground Station

A new amplifier filter for use as a triggering mechanism in the ground station has been constructed. The new system, illustrated in Figure 1, uses the same filter as the old system but utilizes a different input buffer and saturation amplifier. The system incorporates one input from the receiver, two buffered outputs to the delay line and video recorder, and one output to trigger the oscilloscope.

The trigger circuit consists of a low-pass filter and saturation amplifier. The input is fed through a one-transistor buffer to the filter, which is a constant k-pi section with a cutoff frequency of 850 kilocycles. Noise at one megacycle is attenuated by more than twenty decibels. The output of the filter which is terminated in 820 ohms drives the saturation amplifier. The saturation amplifier utilizes two high gain stages of amplification and one buffer output stage. A bias on the input stage of the amplifier can be adjusted so that the amplifier will saturate on an input of 0.2 volts. To eliminate the effects of low-frequency noise, the saturation level can be varied up to 1.2 volts. The output of the saturation amplifier is coupled through a buffer amplifier to the trigger input of the oscilloscope.

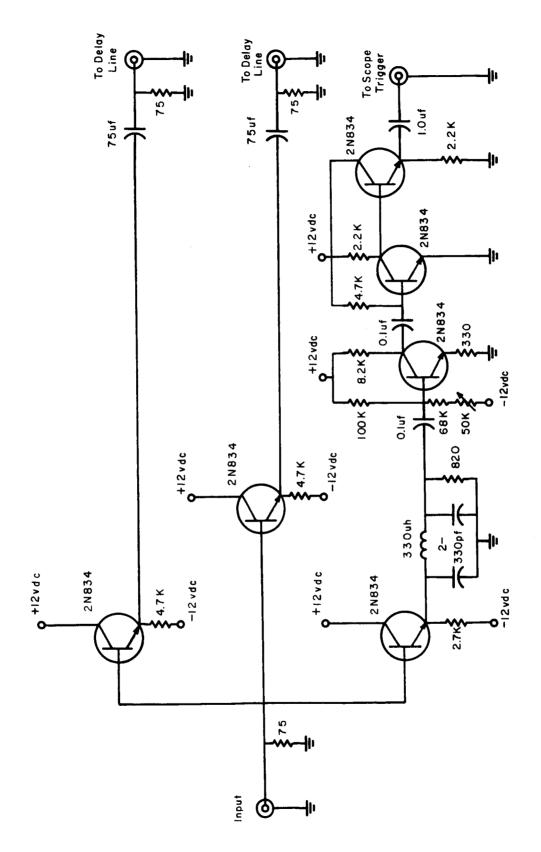


Fig. 1--Circuit Diagram of Ground Station Trigger-Amplifier

Another innovation in the design of the ground station amplifier was to make it a self-contained system. Four 6-volt batteries are utilized to provide the positive and negative 12 wolts necessary for the operation of the amplifier.

Two Phelps-Dodge delay lines provide a 750 nanoseconds delay using type FXA38-75 cable.

An instruction manual for the radar altimeter instrumentation system is being written, Included in this manual are descriptions of the operation, calibration, and maintenance procedure for both the ground station and the missile system.

2. Telemetry Transmitter

Two telemetry transmitters were delivered to the NASA facilities in Huntsville. A block diagram of the units that make up the telemetry transmitter is shown in Figure 2. As shown, this system consists of a Model Six Transmitter and its power supply used in conjunction with a varactor frequency doubler and a bandpass filter.

The two transmitters used were Model Six, Serial Numbers 7 and 14. These transmitters were modified for use in the transmission system and tuned for good pulse response and flat bandwidth.

The varactor doubler uses a Microwave Associates type MA-4060D varactor diode in the single-ended configuration as shown in Figure 3.

A Telonic bandpass filter, model TBP1710-20-3CC1 is employed at the output of the doubler. This filter has an input and output impedance of 50 ohms and an insertion loss of 1.2 db.

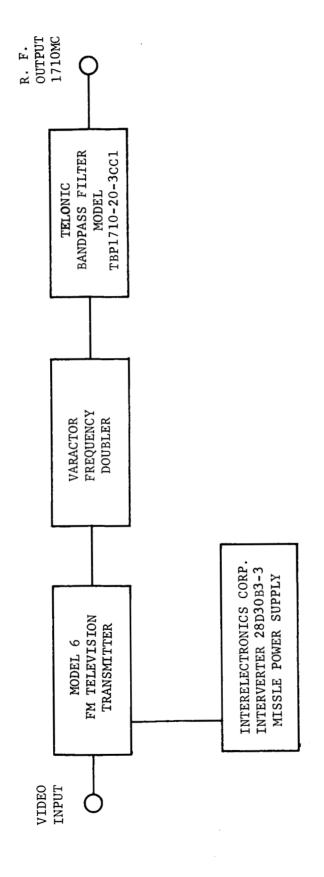
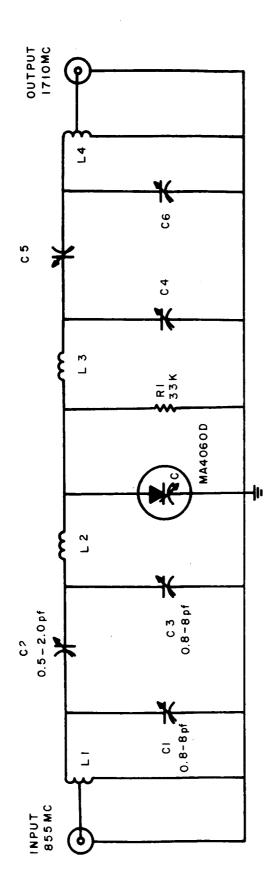


Fig. 2--Block Diagram of Telemetry Transmitter



3.-Varactor Frequency Doubler Used in the Telemetry Transmitter Fig.

B. Television Transmitter

Design work has begun on a solid state 2280 megacycle television exciter unit. A description of the system shown in Figure 4 is given in the following paragraphs.

The video section of the exciter unit consists of a pre-emphasis network and clamping circuit and a broadband video amplifier which is shown in Figure 5. The upper cutoff frequency of the amplifier varies between 20 and 30 megacycles when the value of the simulated load capacitor C4 is varied from 50 pf to 10 pf. The lower cutoff frequency of the amplifier is 20 cycles per second and the mid-band voltage gain is 26 db. Both of these quantities are independent of the value chosen for capacitor C4.

Shunt peaking was employed in the collector circuit of transistor T_1 in order to obtain the 20 to 30 megacycle range of upper cutoff frequency. Without the addition of inductor L1, the upper cutoff frequency varies between five and ten megacycles.

A 2N3375 common-emitter transistor oscillator was designed to operate at 380 megacycles with an output power of one watt. Distributed as well as lumped parameters were used in the design of the circuit. The distributed parameters consisted of four striptransmission line sections. Use of distributed parameters involved special care in the planning of component placement and lead length in order to reduce stray effects.

A schematic diagram of the oscillator circuit is shown in

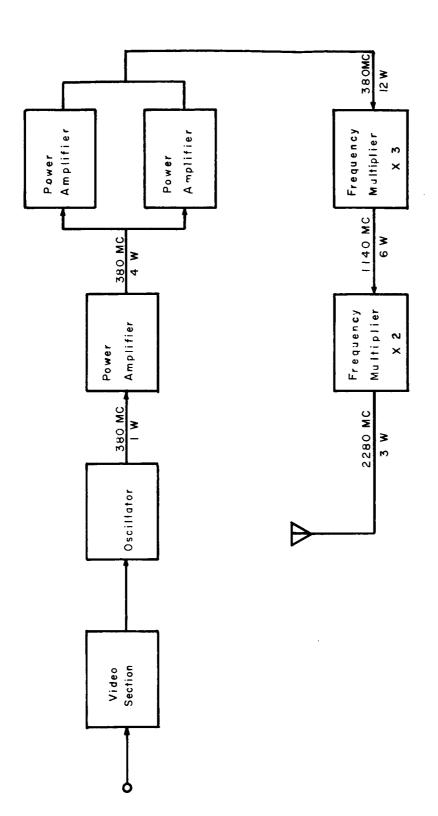


Fig. 4--Block Diagram of Solid-State 2280 Megacycle Television Exciter Unit

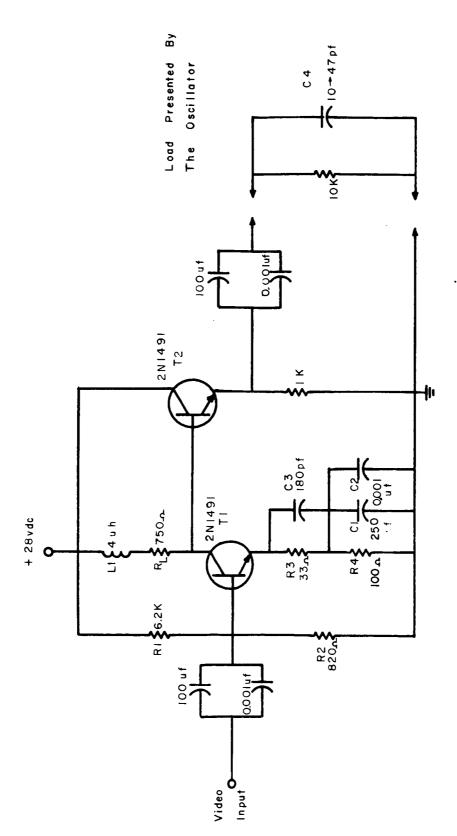


Fig. 5--Circuit Diagram of Video Amplifier

Figure 6. The position of the feedback capacitor C4 is variable along the transmission strips L2 plus L3 and L4 plus L5. Capacitors C1, C2, and C3 are made variable to control the oscillator frequency and output impedance level.

Successful operation of the oscillator was achieved. Since a maximum output power of 6.5 watts was obtainable at the design frequency of 380 megacycles, the one watt design requirement was easily obtained. Over the full range of output power, the efficiency of the oscillator remained near fifty percent for class C operation of the transistor.

Investigation into the bias stability of the oscillator was initiated to determine whether class-A or class-C operation is the most desirable.

An amplifier circuit utilizing two 2N3375 transistors in a parallel-pi connection was designed to produce 12 watts of RF power. Two transistors were used since one transistor was not capable of delivering the required power. A parallel-pi connection was used in order that the input of each transistor could be tuned separately to balance the power demand between the two transistors. The schematic diagram of this amplifier is shown in Figure 7.

The amplifier was designed in two separate stages, input network and output network. Strip transmission line elements having a characteristic impedance of 400 ohms were used in both the input and output networks. Circuit components were obtained using the Smith chart to

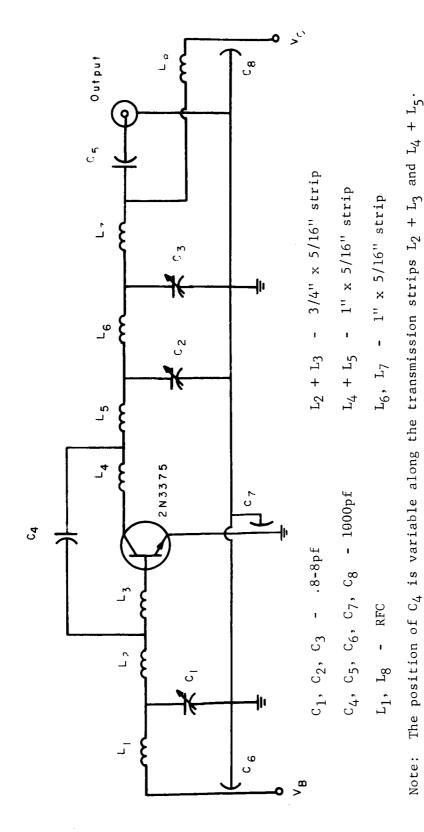
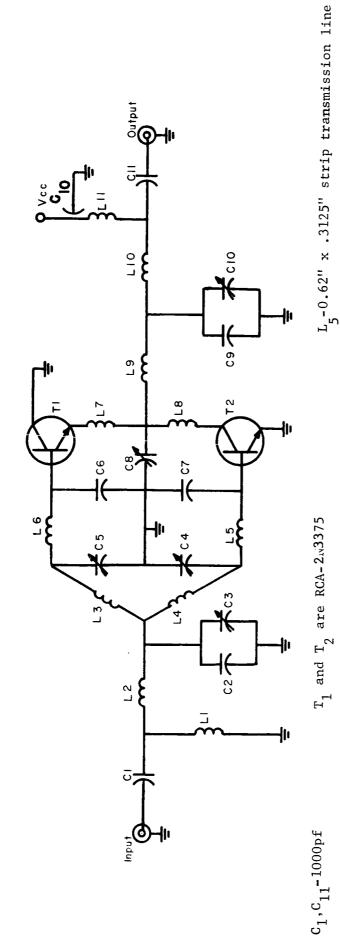


Fig. 6--Circuit Diagram of 380 Megacycle Oscillator



 $^{\rm L}_{\rm 7}, ^{\rm L}_{\rm 8}$ -1.5" x .3125" strip transmission line L_6 -0.60" x .3125" strip transmission line $_{9}^{
m L}$ -1.0" x .3125 strip transmission line L_2 -0.5" x .3125" strip transmission line Vcc = 28 V d.c. L_1, L_{11} -0.2 uh $c_3, c_4, c_5, c_8, c_{10}$ -0.8-8pf

 c_2 -5pf

 c_6 -13pf

C,-16pf

 c_9 -15pf

 $_{10}^{-0.5}$ " x .3125 strip transmission line L_3,L_4 -0175" x .3125" strip transmission line

7--Schematic Diagram of Parallel-Pi Amplifier Fig.

C₁₀-470pf

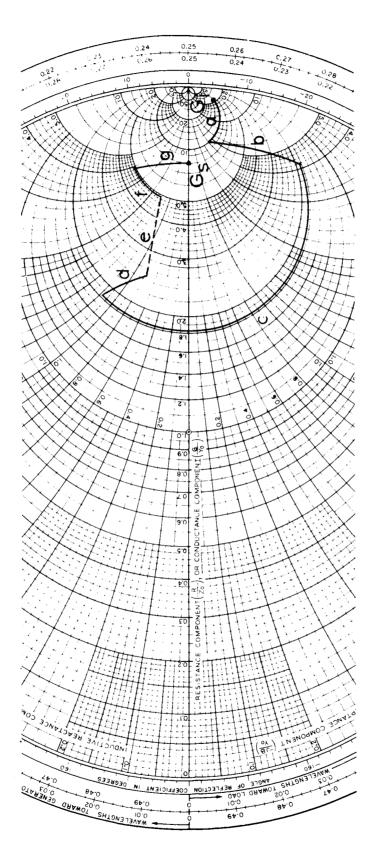
properly match the parameters of the transistors as given by the manufacturer's specifications.

The input network was required to match the parallel input admittance of the transistors to a source impedance of fifty ohms. The matching was accomplished with the Smith chart as shown in Figure 8.

The normalized conductance of the transistor Gi was plotted on the Smith chart, and the proper paths, corresponding to the transmission-line segments and variable capacitors, were taken to reach the point corresponding to the source admittance Gs. Components A, C, and F of the paths shown in Figure 8 correspond to capacitances of 16 pf, 6 pf, and 2.8 pf respectively. Components b, d, and g correspond to 0.6 inch, 0.75 inch, and 0.5 inch line sections respectively. Path e corresponds to the point in the design procedure where the parallel branches are combined to a single input branch.

The output network was required to match the load impedance of fifty ohms to the complex conjugate of the output admittance values of the transistors. Like the input network, the output matching was accomplished with the Smith chart as shown in Figure 9. The normalized load conductance Y_{load} was plotted, and paths, corresponding to line elements and variable capacitances, were taken to reach the point corresponding to the conjugate of the output admittance Y_{out}.

Components a, d, and f were 1.5 inch, 1.0 inch, and 0.5 inch line sections respectively. Components c and e correspond to 8 pf



the input conductance of the transistor and $G_{\rm s}$ is the source conductance. The chart is normalized to the transmission line characteristic admittance of 2.5 millimhos. --Smith chart calculations of the amplifier input network parameters. Fig. 8

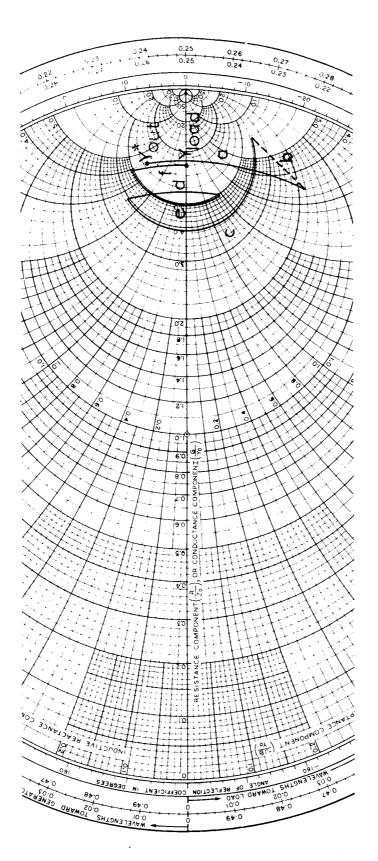


Fig. 9 --Smith chart calculations of the amplifier output network parameters. Y_{10ad} is the load admittance and Y_{put}^* is the conjugate of the output admittance of the transistor. The chart is normalized to the transmission line characteristic admittance of 2.5 millimhos.

and 6 pf capacitances respectively. Path 6 corresponds to the point in the design procedure where the parallel branches are combined into a single output branch.

The above procedure is intended only for initial values in the design. The accuracy of the design procedure is illustrated by the fact that only two additional capacitors were needed to tune the amplifier. A 5.0 pf capacitor was added to path f of the input network and a 15.0 pf capacitor added to path e of the output network. An additional change resulted from the position of the transistor leads in the parallel pi arrangement. The transmission line section to the base of one transistor was shortened by 0.02 inch to keep from overlapping the base pin. Compensation for the shortened line segment was accomplished by reducing the value of the capacitor shunted from the transistor base to ground.

Tests performed on the amplifier indicated that an output of 12 watts can be obtained with a 4 watt input. The collector efficiency at these levels was approximately 50 percent. A picture of the amplifier model is shown in Figure 10.

Multiplication Chain

A multiplication factor of six is required to convert the amplifier frequency of 380 megacycles to the output frequency of 2280 megacycles. To obtain this multiplication, two multiplier stages are being considered. The first stage is a tripler which will convert the amplifier frequency of 380 megacycles to 1140 megacycles. The second stage is a doubler which will convert this 1140 megacycles to the output frequency of 2280 megacycles.

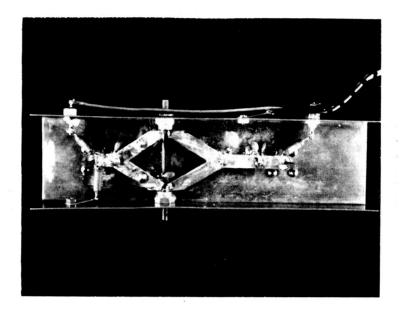


Fig. 10 --Photograph of Parallel-Pi Amplifier Model

A tripler stage using a Microwave Associates type MA-4060D varactor diode was designed and constructed. The circuit diagram of this tripler is shown in Figure 11 and a photograph is shown in Figure 12. The circuit utilizes lumped component techniques in the input and idler sections, and strip-line techniques in the output sections. An efficiency of 60 per cent was obtained. Spurious frequency measurements, referenced to the output, are as follows:

380 mc First Harmonic 45 db down

760 mc Second Harmonic 33 db down

1520 mc Fourth Harmonic 15 db down

The efficiency and harmonic measurements were made using the equipment set-up as shown in Figure 13. The tripler bandpass characteristic was obtained using the equipment shown in Figure 14. This bandpass characteristic is shown in Figure 15. The flat bandwidth is twenty megacycles with a center frequency of 1140 megacycles. All measurements were made with an average power input of two watts.

Design was also intiated on a varactor double stage which will convert the 1140 megacycles output of the tripler to 2280 megacycles.

Two basic circuit configuration are being considered. They are a single ended doubler and a push-pull doubler. The expected efficiency of this doubler stage is 50 per cent.

A minimum efficiency of 25 percent is expected for the multiplier chain. Therefore a minimum power output of three watts for twelve watts of input power is expected.

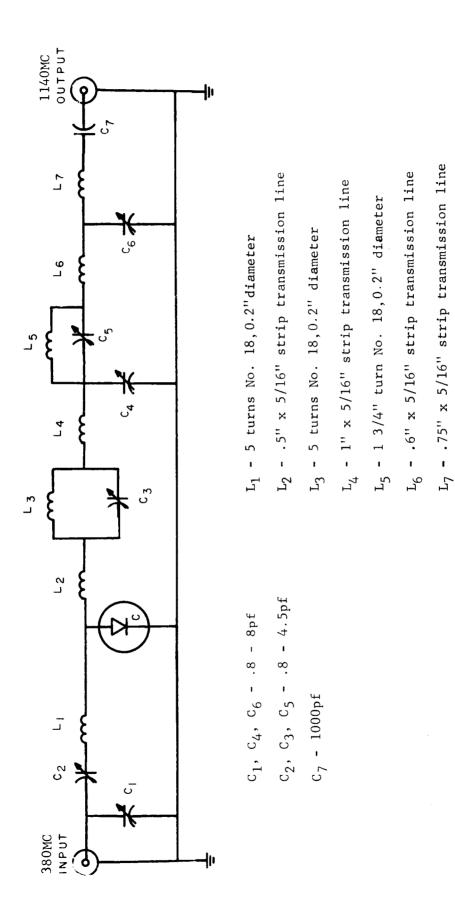


Fig. 11 --Circuit Diagram of Varactor Tripler that Converts 380 Magacycles to 1140 Megacycles

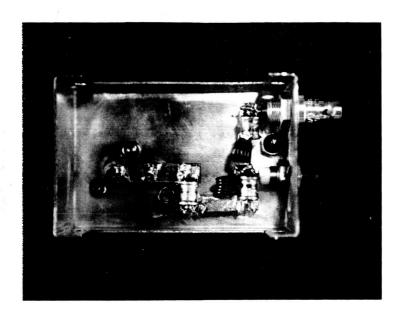


Fig. 12--Photograph of the 380 Megacycle to 1140 Megacycle Varactor Tripler

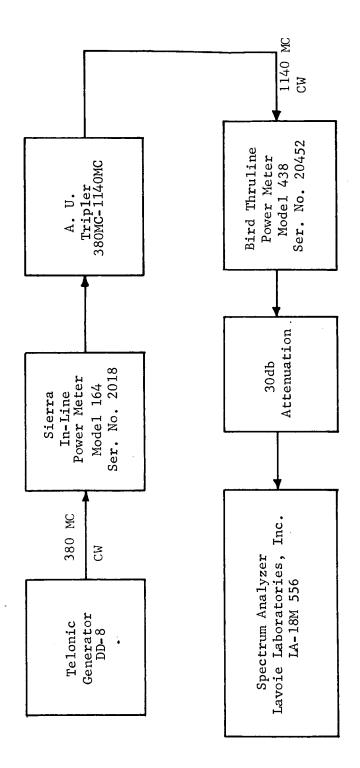


Fig. 13--Block Diagram of the Test Set Up Used to Check the Efficiency and Spurious Harmonic Output of the Varactor Tripler.

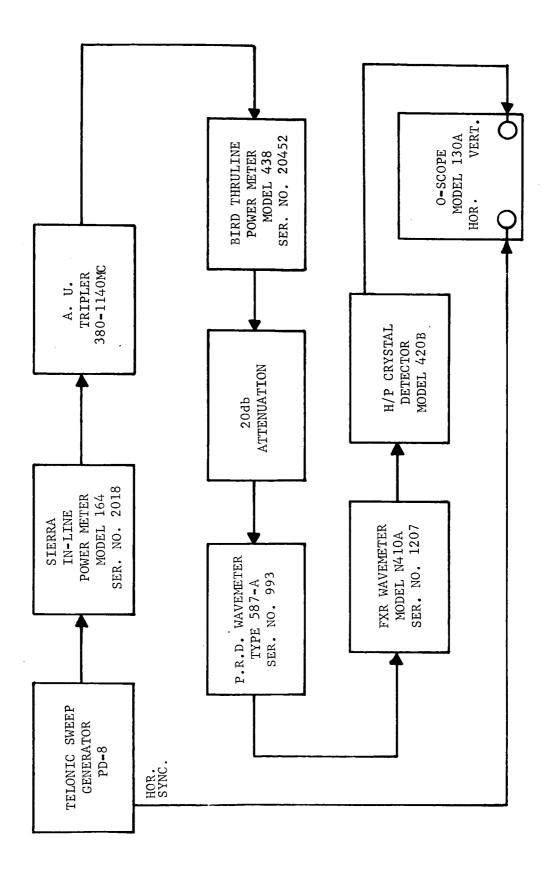


Fig. 14--Block Diagram of Sweep Circuit Used to Sweep the Varactor Tripler

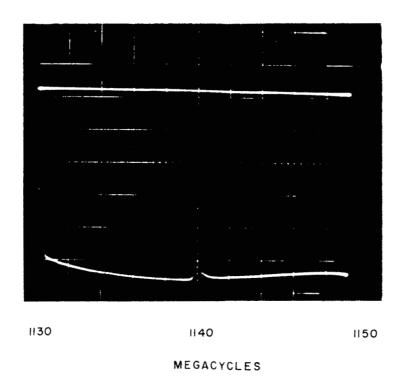


Fig. 15 --Bandpass Characteristic of the Varactor Tripler

A Telonic bandpass filter model TBP 2275-20-3DC, will be placed at the output of the multiplier chain. Specifications on this filter indicate that it has a maximum passband insertion loss of 1.2-db. The transmitter exciter unit is therefore expected to have 2.5 watts of output power at 2280 megacycles.

III. MILLIMETER WAVE STUDY

A study has been conducted to determine the feasibility of placing a system of lenses in each propagation chamber. The lenses, acting as a beam-waveguide, bundle the radiated energy. The otherwise high diffraction losses are thus reduced. It has been decided to construct a system of lenses to verify the results of this study.